WHAT IS CLAIMED IS:

1. A method of creating an integrated circuit device for performing a set of functions, said method comprising:

partitioning said set of functions into (a) a first group of functions to be performed by fixed logic, and (b) a second group of functions to be performed by programmable logic;

obtaining a hardware description language representation of fixed logic for performing said first group of functions;

obtaining a hardware description language representation of said programmable logic;

merging said hardware description language representation of said fixed logic for performing said first group of functions and said hardware description language representation of said programmable logic to create a unified hardware description language representation of said integrated circuit device.

2. The method of claim 1 wherein said unified hardware description language representation defines an integrated circuit device in which said programmable logic is distributed in portions among portions of said fixed logic.

3. The method of claim 1 wherein said obtaining said hardware description language representation of said fixed logic for performing said first group of functions comprises:

designing said first group of functions; and

generating said hardware description language representation of said fixed logic for performing said first group of functions.

4. The method of claim 3 wherein said obtaining said hardware description language

representation of said programmable logic comprises obtaining a preexisting hardware description language representation of said programmable logic.

5. The method of claim 1 wherein said obtaining said hardware description language representation of said fixed logic for performing said first group of functions comprises obtaining a preexisting hardware description language representation of said fixed logic for performing said first group of functions.

6. The method of claim 5 wherein said obtaining said hardware description language representation of said programmable logic comprises obtaining a preexisting hardware description language representation of said programmable logic.

7. The method of claim 1 wherein said obtaining said hardware description language representation of said programmable logic comprises obtaining a preexisting hardware description language representation of said programmable logic.

8. The method of claim 1 further comprising converting said unified hardware description language representation of said integrated circuit device into a physical representation of said integrated circuit device.

9. The method of claim 8 wherein said converting comprises generating a set of at least one mask.

10. The method of claim 8 further comprising fabricating said integrated circuit device from said physical representation.

11. The method of claim 1 wherein said obtaining said hardware description language representation of said programmable logic comprises obtaining a hardware description language representation

of a programmable logic architecture that is optimized for at least one of (a) description by a hardware description language, and (b) fabrication in portions among portions of fixed logic.

12. The method of claim 11 wherein said obtaining a hardware description language representation of a programmable logic architecture comprises obtaining a hardware description language representation of a programmable logic architecture comprising:

an input end;

an output end;

a plurality of tiers of programmable logic elements arranged successively from said input end to said output end, each of said tiers comprising a respective particular number of said programmable logic elements;

a plurality of per-tier conductor channels corresponding in number to said plurality of tiers, wherein:

each per-tier conductor channel is associated with a particular tier,

one of said per-tier conductor channels is closest to said input end and is an input channel, said conductors in said input channel being inputs of said programmable logic architecture,

each particular per-tier conductor channel, other than said input channel, comprises a number of conductors equal to the respective particular number of programmable logic elements in the tier immediately preceding the particular tier with which said particular per-tier conductor channel is associated, and

each conductor in said particular per-tier conductor channel is connected to an output of only one programmable logic element in said tier immediately preceding the particular tier with which said particular per-tier conductor channel is associated;

a plurality of trans-tier conductor channels extending from said input end to said output end intersecting said per-tier conductor channels, wherein:

each said trans-tier conductor channel has a predetermined number of conductors at said input channel,

each said trans-tier conductor channel gains one additional conductor beginning substantially at its respective intersection with each said per-tier conductor channel,

each said programmable logic element communicates with two said trans-tier conductor channels,

inputs of each individual programmable logic element in that one of said tiers at said input end are selected from among conductors in said input channel, and

inputs of each individual programmable logic element in tiers other than that one of said tiers at said input end are selected from among (a) conductors in said per-tier conductor channel with which said tier in which said individual programmable logic element is located is associated, and (b) conductors in both trans-tier conductor channels with which said individual programmable logic element communicates; and

each respective output of said programmable logic architecture is selected from among (a) an output of a respective one of said programmable logic elements other than any of those of said programmable logic elements whose outputs are connected to respective ones of said conductors in said per-tier conductor channels, and (b) a subset of conductors in each of two of said trans-tier conductor channels.

13. A programmable logic architecture comprising:

an input end;

an output end;

a plurality of tiers of programmable logic elements arranged successively from said input end to said output end, each of said tiers comprising a respective particular number of said programmable logic elements;

a plurality of per-tier conductor channels corresponding in number to said plurality of tiers, wherein:

each per-tier conductor channel is associated with a particular tier,

one of said per-tier conductor channels is closest to said input end and is an input channel, said conductors in said input channel being inputs of said programmable logic architecture,

each particular per-tier conductor channel, other than said input channel, comprises a number of conductors equal to the particular number of programmable logic elements in the tier immediately preceding the particular tier with which said particular per-tier conductor channel is associated, and

each conductor in said particular per-tier conductor channel is connected to an output of only one programmable logic element in said tier immediately preceding the particular tier with which said particular per-tier conductor channel is associated;

a plurality of trans-tier conductor channels extending from said input end to said output end intersecting said per-tier conductor channels, wherein:

each said trans-tier conductor channel has a predetermined number of conductors at said input channel,

each said trans-tier conductor channel gains one additional conductor beginning substantially at its respective intersection with each said per-tier conductor channel,

each said programmable logic element communicates with two said trans-tier conductor channels,

inputs of each individual programmable logic element in that one of said tiers at said input end

are selected from among conductors in said input channel, and

inputs of each individual programmable logic element in tiers other than that one of said tiers at said input end are selected from among (a) conductors in said per-tier conductor channel with which said tier in which said individual programmable logic element is located is associated, and (b) conductors in both trans-tier conductor channels with which said individual programmable logic element communicates; and

each respective output of said programmable logic architecture is selected from among (a) an output of a respective one of said programmable logic elements other than any of those of said programmable logic elements whose outputs are connected to respective ones of said conductors in said per-tier conductor channels, and (b) a subset of conductors in each of two of said trans-tier conductor channels.

14. The programmable logic architecture of claim 13 wherein the respective particular number of programmable logic elements in each successive tier, other than that one of said tiers at said input end, is at most equal to the respective particular number of programmable logic elements in an immediately preceding tier.

15. The programmable logic architecture of claim 13 wherein said two of said trans-tier conductor channels, from a subset of the conductors of which said respective output is selected, are the two trans-tier conductor channel with which said respective one of said programmable logic elements communicates.

16. The programmable logic architecture of claim 13 wherein:

there is a one-to-one correspondence between each said programmable logic element and a respective grid point in a two-dimensional array having rows and columns;

each of said tiers contains programmable logic elements that correspond to a respective column of said two-dimensional array;

a respective collection of programmable logic elements including one programmable logic element from each of a plurality of different tiers corresponds to a respective row of said two-dimensional array;

each conductor in a respective one of said per-tier conductor channels connects to programmable logic elements that correspond substantially to one of said columns of said two-dimensional array; and

each conductor in a respective one of said trans-tier conductor channels connects to programmable logic elements that correspond substantially to one of said rows of said two-dimensional array.

17. The programmable logic architecture of claim 16 wherein:

the respective particular numbers of said programmable logic elements in each tier are equal; whereby:

said programmable logic elements collectively map onto a rectangular set of grid points in said two-dimensional array.

18. The programmable logic architecture of claim 16 wherein the respective particular number of said programmable logic elements in any tier other than said one of said tiers at said input end is less than the respective particular number of said programmable logic elements in said immediately preceding tier.

19. The programmable logic architecture of claim 18 wherein the respective particular number of said programmable logic elements in any tier other than said one of said tiers at said input end is one less than the respective particular number of said programmable logic elements in said immediately preceding tier.

20. The programmable logic architecture of claim 19 wherein:

the particular number of said programmable logic elements in that one of said tiers closest to said output end is one; whereby:

said programmable logic elements collectively map onto a triangular set of grid points in said two-dimensional array.

21. The programmable logic architecture of claim 13 wherein each conductor in one said trans-tier conductor channel at said input channel is selectively connectable to a plurality of conductors in said input channel.

22. The programmable logic architecture of claim 21 wherein each conductor in one said trans-tier conductor channel is selectively connectable to each conductor in said input channel.

23. The programmable logic architecture of claim 21 further comprising a respective multiplexer whose output is connected to one of said conductors in said trans-tier conductor channel and whose inputs are connected to said plurality of conductors in said input channel.

24. The programmable logic architecture of claim 13 wherein said one additional conductor is selectively connectable to a plurality of conductors in said per-tier conductor channel at said intersection.

25. The programmable logic architecture of claim 24 wherein said one additional conductor is selectively connectable to each conductor in said per-tier conductor channel at said intersection.

26. The programmable logic architecture of claim 24 further comprising a respective multiplexer whose

output is connected to said additional conductor and whose inputs are connected to said plurality of conductors in said per-tier conductor channel at said intersection.

27. The programmable logic architecture of claim 13 wherein:

each of said programmable logic elements comprises a look-up table having *m* inputs;

for each individual programmable logic element in that one of said tiers at said input end, said *m* inputs are selected from among conductors in said input channel.

28. The programmable logic architecture of claim 27 further comprising a respective multiplexer for selecting said *m* inputs for each respective programmable logic element in that one of said tiers at said input end from among said conductors in said input channel.

29. The programmable logic architecture of claim 13 wherein:

each of said programmable logic elements comprises a look-up table having *m* inputs;

for each respective programmable logic element in a tier other than that one of said tiers at said input end, said *m* inputs are selected from among (a) conductors in said per-tier conductor channel with which said tier in which said individual programmable logic element is located is associated, and (b) conductors in each of said two trans-tier conductor channels with which said individual programmable logic element communicates.

30. The programmable logic architecture of claim 29 further comprising a respective multiplexer for selecting said *m* inputs, for each individual programmable logic element in a tier other than that one of said tiers at said input end, from among (a) conductors in said per-tier conductor channel with which said tier in which said

individual programmable logic element is located is associated, and (b) conductors in each of said two trans-tier conductor channels with which said individual programmable logic element communicates.

31. The programmable logic architecture of claim 13 wherein said subset of conductors in each of said two trans-tier conductor channels comprises, in each of said two trans-tier conductor channels:

one of said predetermined number of conductors that are in said trans-tier conductor channel at said input channel; and

each said additional conductor gained by said trans-tier conductor channel at each of its intersections with said per-tier conductor channels.

32. The programmable logic architecture of claim 31 further comprising a plurality of output multiplexers; wherein:

each of said output multiplexers selects one said output.

33. A programmable logic device constructed according to the architecture of claim 13.

34. A logic device comprising:

at least one portion of fixed logic; and

at least one portion of programmable logic constructed according to the architecture of claim 13.